What is claimed is:

1. A multi-package module comprising a plurality of stacked packages including an upper package and a lower package,

each package comprising:

a board having located on a first side thereof a chip installation area and a bump pad area;

at least one chip disposed in the chip installation area;

a plurality of redistribution patterns formed on the board and electrically connected to the chip;

a plurality of first bump pads formed in the bump pad area which are electrically connected to the redistribution patterns;

a plurality of second bump pads formed on a second side of the board ; and

a plurality of via holes through which the second bump pads are electrically connected to the redistribution patterns,

wherein the respective packages are electrically connected by connecting the second bump pads of the upper of two adjacent packages to the first bump pads of the lower package, the chip installation area of the upper and lower packages not being in vertical alignment with each other.

2. A multi-package module according to claim 1, wherein the chip installation area is positioned on about one half of the first side of the board, and the bump pad area is positioned on about the other one half of the first side of the board.

3. A multi-package module according to claim 1, wherein the second bump pads are formed on the second side of the board in the space corresponding to the chip installation area on the first side of the board.

4. A multi-package module according to claim 1, wherein conductive bumps are provided on the second bump pads electrically connected to the second bump pads of the upper of two adjacent packages to the first bump pads of the lower package.

5. A multi-package module according to claim 1, which further includes an encapsulation member surrounding the chip for protecting the chip from the external environment. .

6. A multi-package module according to claim 5, wherein conductive bumps are provided having similar heights to the height of the encapsulation member.

7. A multi-package module according to claim 1, wherein the second bump pads are formed on substantially the entire second side of the board of the lower package.

8. A multi-package module according to claim 1, further comprising at least one electronic device is disposed on the board of the upper package, and electrically connected to the first bump pads of the upper package.

9. A multi-package module according to claim 4, wherein a portion of the conductive bumps of any two adjacent packages are not in vertical alignment with each other.

10. A multi-package module comprising a plurality of stacked packages including an upper package and a lower package, each package comprising:

a board having located on a first side thereof a chip installation area and a bump pad area;

at least one chip disposed in the chip installation area;

a plurality of redistribution patterns formed on the board and electrically connected to the chip; and

a plurality of first bump pads formed in the bump pad area which are electrically connected to the redistribution patterns,

wherein the respective packages are electrically connected by connecting bump pads of the upper package to bump pads of the lower package, the chip installation area of the upper and lower packages not being in vertical alignment with each other.

11. A multi-package module according to claim 10, which further includes an encapsulation member surrounding the chip for protecting the chip from the external environment.

12. A multi-package module according to claim 10, wherein the chip installation area is positioned on about one half of the first side of the board, and the bump pad area is positioned on about the other one half of the first side of the board.

13. A multi-package module according to claim 11, wherein conductive bumps are provided having similar heights to the height of the encapsulation member.

14. A multi-package module according to claim 10, wherein at least one electronic device is disposed on the board of the upper package, and is electrically connected to the first bump pads of the upper package.

15. A multi-package module according to claim 10, wherein a plurality of second bump pads are formed on a second side of the board, and a plurality of via holes through which the second bump pads are electrically connected to the redistribution patterns.

16. A multi-package module according to claim 15, wherein the packages are electrically connected by connecting the second bump pads of the upper of two adjacent packages to the first bump pads of the lower package.

17. A multi-package module according to claim 15, wherein the second bump pads are formed on the second side of the board in the space corresponding to the chip installation area on the first side of the board.

18. A multi-package module according to claim 15, wherein conductive bumps are provided on the second bump pads for electrically connecting the second bump pads of the upper package to the first bump pads of the lower package.

19. A multi-package module according to claim 15, wherein the second bump pads are formed on substantially the entire second side of the board of the lower package.

20. A multi-package module comprising a plurality of stacked packages including an upper package and a lower package, each package comprising:

a board having located on one side thereof a chip installation area and a bump pad area;

at least one chip disposed in the chip installation area chip; and

a plurality of first bump pads formed in the bump pad area electrically connected to chip,

wherein the respective packages are electrically connected by connecting bump pads of the upper package to bump pads of the lower package, the chip installation area of the upper and lower packages being laterally offset from each other.